REMARKS

The outstanding issues in the instant application are as follows:

- Claims 1-4 and 6-48 are rejected under 35 U.S.C. § 112, ¶1, as not being enabled.

- Claims 1-4 and 6-48 are rejected under 35 U.S.C. § 103(a).

Applicant hereby traverses the outstanding rejections, and requests reconsideration and withdrawal in light of the amendments and remarks contained herein. Claims 1-4 and 6-49 are pending in this application.

AMENDMENTS

Claim 1 was amended to include "one or more filters, and wherein said one or more filters comprise only first order filters, second order filters, or a combination thereof" Support for this amendment can be found in the Specification, Drawings, and Original Claims, for example in paragraphs 0031-0032, Figure 2B, and Original Claims 6-7, 19, 32, 35, 41, and 47. No new matter was added. The Examiner has repeatedly commented that the phrase "first order filter" is not used in the Specification. *See, e.g.,* Office Action at 7. As the phrase "first order filter" appears repeatedly in the Original Claims, the written description requirement is satisfied as to "first order filter." *See* M.P.E.P. § 2163 ("It is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification."). Additionally, "[t]he subject matter of the claim need not be described literally (i.e., using the same terms or in haec verba) in order for the disclosure to satisfy the description requirement." *See* M.P.E.P. § 2163.02. Rather, "the fundamental factual inquiry [for the written description requirement] is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed." *See id.* This may be shown "using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention." *See id.* At least Figure 2B clearly shows a filter network utilizing "one or more filters, and wherein said one or more filters comprise only first order filters, second

order filters, or a combination thereof." The terms "first order filter" and "second order filter" are well-known to those skilled in the art. Attached as Exhibit 1 are excerpts from an introductory college circuits book defining first order circuits (pages 241-243) and second order circuits (pages 306-307). *See* Exhibit 1, Nilsson and Riedel, ELECTRIC CIRCUITS (1996). Thus, the Specification and Drawings illustrate to those skilled in the art that the Applicants were in possession of the idea as now claimed at the time of the invention.

Claim 2 was amended to include the limitation "wherein said filter network does not require manual tuning or adjustment." Support for this amendment can be found in the Specification and Drawings, for example in paragraphs 0031-0032 and Figure 2B. No new matter was added.

Claim 3 was amended to incorporate the limitations previously included in Original Claim 2. Support for this amendment can be found in the Specification, Drawings, and original claims, for example Original Claim 2. No new matter was added.

Claim 17 was amended to simplify the "filter network element" and to make clear that the signal stream as converted "is substantially without said additional signal energy." Support for this amendment can be found in the Specification and Drawings, for example in paragraphs 0031-0032 and Figure 2B. No new matter was added.

Claim 21 was amended to include the limitation "wherein said first and said second filters ... do not require manual tuning or adjustment." Support for this amendment can be found in the Specification and Drawings, for example in paragraphs 0031-0032 and Figure 2B. No new matter was added.

Claim 29 was amended to include the step of "filtering said signal stream with a filter network utilizing one or more filters, wherein said one or more filters comprise only first order filters, second order filters, or a combination thereof." Support for this amendment can be found in the Specification, Drawings, and Original Claims, for example in paragraphs 0031-0032, Figure 2B, and Original Claims 6-7, 19, 32, 35, 41, and 47, as explained above with respect to Claim 1. No new matter was added.

Claim 34 was amended to include the step of "filtering said signal stream with one or more filters, wherein said one or more filters comprise only first order filters, second order filters, or a combination thereof, and wherein said one or more filters do not require manual tuning or adjustment, said filtering to provide relatively coarse filtering of said application signal." Support for this amendment can be found in the Specification, Drawings, and Original Claims, for example in paragraphs 0031-0032, Figure 2B, and Original Claims 6-7, 19, 32, 35, 41, and 47, as explained above with respect to Claim 1. No new matter was added.

Claim 39 was amended to simplify the "filtering" step. Support for this amendment can be found in the Specification and Drawings, for example in paragraphs 0031-0032 and Figure 2B. No new matter was added.

Claim 46 was amended to include the step of "filtering said signal stream utilizing one or more filters to provide approximately 20 dB of filtering of said forward application terminal, wherein said one or more filters comprise only first order filters, second order filters, or a combination thereof and said filters do not require manual tuning or adjustment." Support for this amendment can be found in the Specification, Drawings, and Original Claims, for example in paragraphs 0031-0032, Figure 2B, and Original Claims 6-7, 19, 32, 35, 41, and 47, as explained above with respect to Claim 1. No new matter was added.

Claim 49 was added, dependant on Claim 29, having the limitation "wherein said filter network does not require manual tuning or adjustment." Support for this amendment can be found in the Specification and Drawings, for example in paragraphs 0031-0032 and Figure 2B. No new matter was added.

I. REJECTION UNDER 35 U.S.C. § 112, ¶ 1 – Enablement Requirement

Claims 1-4 and 6-48 are rejected under 35 U.S.C. § 112, ¶1, as not being enabled. Each claim includes or depends from a claim including the limitation "low order filter." Claims 6-7, 19-22, 32, 35, 41, and 47 are also rejected under the same basis where each claim includes or depends from a claim having the phrase "first order filter." Applicants respectfully traverse these rejections at least because the phrases "first order filter" and

"second order filter" are both well-known to those skilled in the art and specifically taught in the Applicants' Application.

"The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." M.P.E.P. § 2164 (quoting *United States v. Telectronics, Inc.*, 857 F.2d 778, 785 (Fed. Cir. 1988)). "A patent need not teach, and preferably omits, what is well known in the art." *Id.* (citing *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991)).

Although Applicants assert that the phrase "low order filter" meets the enablement requirement of § 112, ¶1, Applicants have amended the phrase "low order filter" to expressly recite "first order filter" and "second order filter." Both of these phrases are well-known to those skilled in the art. *See* Exhibit 1, Nilsson and Riedel, ELECTRIC CIRCUITS (excerpts from an introductory college circuits book defining first order circuits (pages 241-243) and second order circuits (pages 306-307)). As such, these terms meet the enablement requirement of § 112, ¶1. *See* M.P.E.P. § 2164.

Applicants additionally note that the Examiner repeatedly stated that the phrase "first order filter" (and "second order filter") was not used in the specification. Applicants respectfully note that there is no requirement that claim language be literally included in the specification in order to meet the enablement requirement of § 112, ¶ 1, and where the teachings are well-known in the art as here, such description is preferably omitted. *See* M.P.E.P. at § 2164. Regardless, the Specification, Drawings, and Original Claims in the Application specifically teach building first order filters and second order filters. For example, Figure 2B specifically illustrates examples of second order filters and Original Claims 6-7, 19, 32, 35, 41, and 47 teach the use of first order filters. Thus, Applicants assert that Claims 1-4 and 6-48 as amended meet the enablement requirement of § 112, ¶ 1 and respectfully request that the Examiner withdraw the rejections.

REJECTIONS UNDER 35 U.S.C. § 103(a)

In order to establish obviousness under 35 U.S.C. § 103(a), three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the references or combine reference teachings. Second, there must be a reasonable expectation of success. Third, the applied art must teach or suggest all the claim limitations. M.P.E.P. § 2143.03. Applicants assert that the rejections do not satisfy these criteria, as discussed below.

II. Rejection of Claims 1, 6-11, 15-19, 21-22, 25-26, 29-32, 34-35, 39, 41-42 and 46-48 over Bertonis et al in view of Rogers et al

Claims 1, 6-11, 15-19, 21-22, 25-26, 29-32, 34-35, 39, 41-42 and 46-48 are rejected under § 103(a) over U.S. Patent No. 6,625,222 to Bertonis et al (hereinafter *Bertonis*) in view of U.S. Patent No. 6,681,103 to Rogers et al (hereinafter *Rogers*). Applicants respectfully traverse these rejections.

A. Independent Claims 17 and 39

1. *Bertonis does not teach a tuner for rejecting an image frequency substantially greater in amplitude than the signal of interest*

Bertonis does not teach all claim limitations of Claims 17 and 39 because neither *Bertonis* nor *Rogers* teaches systems and methods for filtering with filters and mixing with an image reject mixer a signal stream "wherein said image frequency signal as provided to said tuner circuit is substantially greater in amplitude than said signal of interest" to obtain the signal of interest "substantially without said image frequency signal." Claims 17 and 39 claim an apparatus and method respectively for accepting a signal where the image frequency signal is substantially greater in amplitude than the signal of interest and processing the signal to produce a signal substantially without the image frequency signal. *Bertonis* does not teach processing a signal with such difficult characteristics. Indeed, *Bertonis* merely teaches the use of the filter network and image reject mixer of Figure 8 to select the copy of a signal having better quality where two copies of a signal are transmitted in upper and lower sidebands resulting from a single upconversion. *See Bertonis* at col. 9, lns. 47-53. Thus, the

signal rejected is not "substantially greater in amplitude" than the signal of interest, but is in fact approximately the same amplitude and likely less than the signal of interest.

2. Lack of Motivation

Applicants assert that there is no motivation either in the references or in what each reference suggests to combine the image reject mixer of *Bertonis* with the filter network of *Rogers* because *Bertonis* teaches a filter network with low-pass and bandpass filters, while *Rogers* teaches a notch filter and *Rogers* discouraged the use of image reject ***mixers*** as not offering satisfactory performance. Figure 8 of *Bertonis* teaches the use of two low-pass filters 93 and 94, as well as a band-pass filter 99 for filtering a signal prior to reaching an image reject mixer.[1] *Rogers* teaches the use of a notch filter/amplifier in its filter network. *See Rogers* at col. 2, lns. 24-39. The notch filter taught in *Rogers*, by definition, rejects signals around a certain frequency (here, an image frequency) and allows signals above and below that frequency to pass. In contrast, a low pass filter, by definition, passes signals below a frequency and blocks those above that frequency, while a band pass filter, by definition, allows signals within a frequency band to pass while blocking signals above and below that frequency. One skilled in the art would not be motivated to substitute the notch filter of *Rogers* into the low pass filters 93 and 94 or band pass filter 99 of *Bertonis* because the notch filter of *Rogers* would not carry out the functional filtering taught by *Bertonis*. Further, *Bertonis* teaches reliance on a image reject mixer to reject an image frequency and thus does not require a notch filter.

The Examiner states that *Rogers* teaches "an image reject ***filter*** (figure 1) having a filter network (see FILTER figure 1) coupled to said image reject mixer (see MIXER figure 1)." *See, e.g.,* Office Action at page 7 (emphasis added). Applicants assert that this characterization of *Rogers*' teaching is incorrect. *Rogers*' Figure 1 illustrates a prior art superheterodyne receiver having a typical low noise amplifier (LNA), an image reject ***filter***, and a mixer. *Rogers*, Col. 1, lns. 11-22. The mixer depicted in Figure 1 of *Rogers* is not

[1] It should be noted that the Applicants contend, as will be discussed in detail later, that low pass filters 93 and 94, which have been asserted as meeting the filter network claimed in the Application, are actually part of the image reject mixer 105 and thus cannot constitute a separate filter network. The Applicants, however, direct the Examiner to band pass filter 99 as providing the closest analog in Figure 8 of *Bertonis* to the claimed filter.

described to be an image reject ***mixer***. As *Rogers* explains further in column 1, image reject filters have typically been implemented using more-costly off-chip filters, such as surface acoustic wave (SAW) filters. *See Rogers* at col. 1, lns. 35-53. *Rogers* explains that on-chip image reject filters have previously not been shown to be effective, so the only effective on-chip image rejection has previously been achieved through image reject ***mixers***. *See id.* at col. 1, lns. 61-67. This explanation from *Rogers* is important because *Rogers* teaches that the level of image rejection achieved with image reject mixers is not satisfactory. *See id.* at col. 1, lns. 62-65. Therefore, in lieu of including such image reject mixers in a receiver, *Rogers* teaches the use of an on-chip notch filter added to an LNA or other standard component to perform image rejection. *See id.* at col. 2, lns. 24-30. Thus, one of ordinary skill in the art would not look to *Rogers*, which teaches away from image rejection via an image reject mixer, to take the image reject filter of *Rogers* and combine it with an image reject mixer as arguably described in *Bertonis*. No where in either *Bertonis* or *Rogers* or in what either suggests does it support combining the image reject notch ***filter*** taught in *Rogers* with an image reject ***mixer***.

Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Independent Claims 17 and 39 be withdrawn.

B. Independent Claims 1, 29, 34, and 46

1. *Bertonis does not teach a filter network utilizing only first order filters and second order filters*

Bertonis does not teach the use of any specific type of filter network, and thus does not teach a filter network utilizing only first order filters and second order filters. The Examiner points to items 93 and 94 in Figure 8 of *Bertonis* as teaching a "first order used to perform Low Pass Filtering." *See* Office Action at 7. As a preliminary matter, items 93 and 94 are part of image reject mixer 105 and could thus not be a filter network separate from the image reject mixer. However, Applicants direct the Examiner to RF Filter 99 also in Figure 8. As discussed above with regard to the § 112 rejection, it is well known to those skilled in

Because neither low pass filters 93 and 94 nor band pass filter 99 provide a motivation to combine these black-

the art that a "first order filter" and a "second order filter" are specific types of filters. *See, e.g.* Exhibit 1. *Bertonis* do not teach that RF Filter 99 (or Low Pass Filters 93 and 94) in Figure 8 are any specific type of filter; they are merely black box filters without any particular characteristics. The specification of *Bertonis* does not describe RF Filter 99 (or Low Pass Filters 93 and 94) in any further detail. *See, e.g. Bertonis* at col. 9, lns. 54-61. As explained in Applicants' Specification, typical prior art filter networks utilized complicated filter arrangements (i.e., more complicated than first and second order filters) and/or tuneable components in order to obtain sharp filtering responses. *See* Specification at 0024-0025. *Bertonis* contains no teaching differentiating its invention from this prior art approach. As such, *Bertonis* does not teach a filter network or filtering utilizing "only first order filters and second order filters" as claimed in Claims 1, 29, 34, and 46.

2. Lack of Motivation

Applicants assert that there is no motivation either in the references or in what each reference suggests to combine the image reject mixer of *Bertonis* with the filter network of *Rogers* because *Bertonis* teaches a filter network with low-pass and bandpass filters, while *Rogers* teaches a notch filter and *Rogers* discouraged the use of image reject ***mixers*** as not offering satisfactory performance. As discussed above, the Examiner has pointed to two low-pass filters 93 and 94 in Figure 8 in *Bertonis*, while the Applicants have pointed to a band-pass filter 99 as the closest analog to the filter network of the Applicant's Claims. *Rogers* teaches the use of a notch filter/amplifier in its filter network. *See Rogers* at col. 2, lns. 24-39. The notch filter taught in *Rogers*, by definition, rejects signals around a certain frequency (here, an image frequency), and allows signals above and below that frequency to pass. In contrast, a low pass filter, by definition, passes signals below a frequency and blocks those above that frequency, while a band pass filter, by definition, allows signals within a frequency band to pass while blocking signals above and below that frequency. One skilled in the art would not be motivated to substitute the notch filter of *Rogers* into the low pass filters 93 and 94 or band pass filter 99 of *Bertonis* because the notch filter of *Rogers* would not carry out the functional filtering taught by *Bertonis*. Further, *Bertonis* teaches reliance on a image reject mixer to reject an image frequency and thus does not require a notch filter.

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box filters with the filters taught in *Rogers*, Applicants choose to discuss all three for sake of completeness.

The Examiner states that *Rogers* teaches "an image reject ***filter*** (figure 1) having a filter network (see FILTER figure 1) coupled to said image reject mixer (see MIXER figure 1)." *See, e.g.,* Office Action at page 7 (emphasis added). Applicants assert that this characterization of *Rogers*' teaching is incorrect. *Rogers*' Figure 1 illustrates a prior art superheterodyne receiver having a typical low noise amplifier (LNA), an image reject ***filter***, and a mixer. *Rogers*, Col. 1, lns. 11-22. The mixer depicted in Figure 1 of *Rogers* is not described to be an image reject ***mixer***. As *Rogers* explains further in column 1, image reject filters have typically been implemented using more-costly off-chip filters, such as surface acoustic wave (SAW) filters. *See Rogers* at col. 1, lns. 35-53. *Rogers* explains that on-chip image reject filters have previously not been shown to be effective, so the only effective on-chip image rejection has previously been achieved through image reject ***mixers***. *See id.* at col. 1, lns. 61-67. This explanation from *Rogers* is important because *Rogers* teaches that the level of image rejection achieved with image reject mixers is not satisfactory. *See id.* at col. 1, lns. 62-65. Therefore, in lieu of including such image reject mixers in a receiver, *Rogers* teaches the use of an on-chip notch filter added to an LNA or other standard component to perform image rejection. *See id.* at col. 2, lns. 24-30. Thus, one of ordinary skill in the art would not look to *Rogers*, which teaches away from image rejection via an image reject mixer, to take the image reject filter of *Rogers* and combine it with an image reject mixer as arguably described in *Bertonis*. No where in either *Bertonis* or *Rogers* or in what either suggests does it support combining the image reject notch ***filter*** taught in *Rogers* with an image reject ***mixer***.

Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Independent Claims 1, 29, 34, and 46 be withdrawn.

C. Independent Claims 34 and 46

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 34 and 46, as amended, because *Bertonis* does not teach first order filters or second order filters and *Rogers* does not teach filters that do not require manual tuning. In addition

to the limitations discussed above with respect to each of the independent claims, Claims 34 and 46 claim first order filters and second order filters that "do not require manual tuning or adjustment." As discussed above, *Bertonis* does not teach first order filters or second order filters. *Rogers* teaches the use of tunable filters in order "to overcome variations in device parameters." *See Rogers* at col. 5 lns. 42-48. Thus, the combination of *Bertonis* and *Rogers* does not teach all the claim limitations of Claims 34 and 46. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Independent Claims 34 and 46 be withdrawn.

D. Dependent Claims 2, 21, 42, and 49[2]

Claims 2, 21, 42, and 49each depend either directly or indirectly from Independent Claims 1, 17, 29, and 39 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, 29, and 39 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 2, 21, 42, and 49, as amended, because *Bertonis* does not teach first order filters or second order filters and *Rogers* does not teach filters that do not require manual tuning. Each of Claims 2, 21, 42, and 49 claim first order filters and second order filters that "do not require manual tuning or adjustment." As discussed above, *Bertonis* does not teach first order filters or second order filters and *Rogers* teaches only tunable filters. *See Rogers* at col. 5 lns. 42-48. Thus, neither *Bertonis* nor *Rogers* teach the use of first order filters and second order filters where the filters do not require manual tuning. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 2, 21, 42, and 49 be withdrawn.

[2] It should be noted that each of Claims 2, 20, 32, and 42 has been amended to remove previous limitations and a limitation of first order filters and second order filters that "do not require manual tuning or adjustment." As such, pending rejections as to these claims are moot. For example, Claim 2 was rejected over *Bertonis* in view of *Rogers* in further view of *Cheah* based on a limitation "wherein signal energy of said data channel is approximately 20 dB lower in amplitude than said image frequency signal energy." As this limitation has been removed, the pending rejection is moot.

E. Dependent Claims 6-7, 19, 31-32, 35, 41, and 47

Claims 6-7, 19, 31-32, 35, 41, and 47 each depend either directly or indirectly from Independent Claims 1, 17, 29, 34, 39, and 46 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, 29, 34, 39, and 46 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 6-7, 19, 31-32, 35, 41, and 47 because neither *Bertonis* nor *Rogers* teach the specific filter configurations claimed by Claims 6-7, 19, 31-32, 35, 41, and 47. As discussed above, *Bertonis* does not teach first order filters or second order filters, but teaches only a black box RF filter leading to an image reject mixer. *See Bertonis* at Figure 8. *Rogers* teaches a specific notch filter design to be used in conjunction with a low noise amplifier. *See Rogers* at Figures 3-4. Thus, neither *Bertonis* nor *Rogers* teach the particular filter designs and methods claimed in Claims 6-7, 19, 31-32, 35, 41, and 47. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 6-7, 19, 31-32, 35, 41, and 47 be withdrawn.

F. Dependent Claims 9-10, 22, and 25

Claims 9-10, 22, and 25 each depend either directly or indirectly from Independent Claims 1 and 17 and are thus likewise believed to be allowable at least based on their dependency from Claims 1 and 17 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 9-10, 22, and 25 because *Bertonis* does not teach an image reject mixer implemented with integrated circuit technology and *Rogers* does not teach an image reject mixer. While the Examiner asserts that *Bertonis* "does show IC technology being employed," Applicants respectfully note that the Examiner has provided no citation for this assertion. Office Action at 9. Applicants also note that a review of *Bertonis* did not reveal any reference to the use of integrated circuit technology to implement various components as claimed in Claims 9-10,

22, and 25. Additionally, *Rogers* specifically rejects the use of an image reject mixer. *See Rogers* at col. 1, lns. 61-67. Thus, neither *Bertonis* nor *Rogers* teaches an image reject mixer implemented with integrated circuit technology as used in combination with the claimed elements. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 9-10, 22, and 25 be withdrawn.

G. Dependent Claims 11, 18, and 48

Claims 11, 18, and 48 each depend either directly or indirectly from Independent Claims 1, 17, and 46 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, and 46 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 11, 18, and 48 because neither *Bertonis* nor *Rogers* teaches the claimed apparatuses and methods adapted to process the signal described in Claims 11, 18, and 48. The Examiner asserts that *Bertonis* "teaches that Image and desired signals are closely (i.e. 10%) spaced" and cites to col. 2 lns. 5-8. *See* Office Action at 9. Applicants note that Claims 11, 18, and 48 do not claim a signal where "Image and desired signals are closely (i.e., 10%) spaced," but rather claims apparatuses and methods for processing such a signal. As an example, Claim 11 is produced below integrated into Claim 1 from which it depends with the limitation of Claim 11 underlined:

> 11. A data channel tuner comprising:
> an input interface for accepting said data channel, wherein said input interface further accepts signal energy at a frequency associated with an image of said data channel as mixed by said tuner, <u>wherein said image frequency signal energy is at a frequency approximately 10% removed from a frequency of said data channel;</u>
> a filter network coupled to said input interface, wherein said filter network utilizes only first order filters and second order filters; and
> an image reject mixer coupled to said filter network and providing frequency conversion of said data channel.

Thus, Claim 11 does not merely claim the data channel tuner of Claim 1 and a signal, but rather claims a data channel tuner comprising an input interface for accepted the signal as claimed in Claim 11.

Applicants note that the signal described in col. 2, lns. 5-8 and cited by the Examiner is not the signal accepted by Figure 8 of *Bertonis*, which the Examiner has asserted teaches other elements of the invention. Indeed, in the portion cited by the Examiner, *Bertonis* describes a prior art signal, MMDS, and explains that it is disfavored because the close signals require cumbersome processing equipment. *See Bertonis* col. 1, ln. 53 – col. 2, ln. 18. *Bertonis* the goes on to teach a different signal – an upconverted version of a signal generated by a standard cable modem – for use with the invention, including Figure 8. *See id.* at col. 2 ln. 55 – col. 3 ln. 40. Indeed, *Bertonis* merely teaches the use of the filter network and image reject mixer of Figure 8 to select the copy of a signal having better quality where two copies of a signal are transmitted in upper and lower sidebands resulting from a single upconversion. *See id.* at col. 9, lns. 47-53. Such signal processing is different than that claimed in the Application. Thus, *Bertonis* does not teach the hardware of Figure 8 being used to handle signals "wherein said image frequency signal energy is at a frequency approximately 10% removed from a frequency of said data channel."

2. *Lack of Motivation to Combine*

The Examiner has offered no motivation to combine these two disparate teachings and none exists. As discussed above, *Bertonis* teaches using the hardware of Figure 8 with upconverted version of a signal generated by a standard cable modem in the "2.40 – 2.4835 GHz" range. *See* col. 2, ln. 55 – col. 3, ln. 40. In a completely separate discussion, *Bertonis* mentions a prior art signal, MMDS, and explains that it is disfavored because the close signals require cumbersome processing equipment. *See Bertonis* col. 1, ln. 53 – col. 2, ln. 18. The Examiner has pointed to the MMDS teaching as rendering Claims 11, 18, and 48 obvious. However, *Bertonis* does not provide any motivation to adapt the hardware of Figure 8 to accommodate a MMDS signal or any other signal other than that specified. To the contrary, *Bertonis* teaches away, noting that utilizing a MMDS signal is disfavored based on the complicated hardware required to handle the signal and goes on to teach the use of the signal described in conjunction with Figure 8. *See id.* Thus, there is no motivation to adapt

the teachings of Figure 8 to accommodate a MMDS signal or any other signal. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 11, 18, and 48 be withdrawn.

H. Dependent Claims 15-16, 26, and 30

Claims 15-16, 26, and 30 each depend either directly or indirectly from Independent Claims 1, 17, and 29 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, and 29 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* does not teach all claim limitations of Claims 15-16, 26, and 30 because none of the references teach the claimed apparatuses and methods adapted to process the signal as described in Claims 15-16, 26, and 30. Each of Claims 15-16, 26, and 30 limits the claimed apparatus or process from which it depends by imposing a requirement that the apparatus or process be capable of processing an incoming signal having certain characteristics. The fact that these characteristics are defined (such as by the OPENCABLE standard as described in the Specification at 0006) does not in any way teach or render obvious apparatuses and methods for meeting processing these signals. Indeed, *Bertonis* merely teaches the use of the filter network and image reject mixer of Figure 8 to select the copy of a signal having better quality where two copies of a signal are transmitted in upper and lower sidebands resulting from a single upconversion. *See Bertonis* at col. 9, lns. 47-53. Such signal processing is different than that claimed in the Application. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 15-16, 26, and 30 be withdrawn.

III. Rejection of Claims 3-4, 12-14, 20, 23-24, 27-28, 33, 37-38, 40, 43-45 over Bertonis et al in view of Rogers et al in Further view of Cheah or Applicants' Admittance

Claims 3-4, 12-14, 20, 23-24, 27-28, 33, 37-38, 40, 43-45 are rejected under § 103 over *Bertonis* in view of *Rogers* in further view of U.S. Patent No. 6,674,409 to Cheah (hereinafter *Cheah*) or Applicants' own admittance. Applicants respectfully traverse these rejections.

A. Dependent Claims 3-4, 20, 23-24, 33, 36-38, 40, and 44-45

Claims 3-4, 23-24, 33, 36-38, 40, and 44-45 each depend either directly or indirectly from Independent Claims 1, 17, 29, 34, and 39 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, 29, 34, and 39 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* in further view of Applicant's Admittance or *Cheah* does not teach all claim limitations of Claims 3-4, 20, 23-24, 33, 36-38, 40, and 44-45 because none of the references teach the claimed apparatuses and methods adapted to process the signals as described in Claims 3, 23, 33, and 36 or to meet the performance requirements as described in Claims 3-4, 24, 37-38, 40, and 44-45. Each of these claims limits the claimed apparatus or process from which it depends by imposing a requirement that the apparatus or process be capable of (a) processing an incoming signal possessing certain signal-to-noise characteristics (*see, e.g.* Claim 23), (b) produce a certain amount of noise rejection (*see, e.g.* Claim 4), or (c) produce an output signal having defined signal to noise and distortion value (*see, e.g.* Claim 24). The fact that a performance standard is defined (such as by the OPENCABLE standard as described in the Specification at 0006) does not in any way teach or render obvious apparatuses and methods for meeting these performance standards. Thus, the existence of performance standards (as taught in the Specification and *Cheah*) does not teach or render obvious apparatuses or methods meeting those performance standards. *Bertonis* does not teach apparatuses or methods adapted to meet the performance standards claimed in Claims 3-4, 24, 37-38, 40, and 44-45. Indeed, *Bertonis* merely teaches the use of the filter network and image reject mixer of Figure 8 to select the copy of a signal having better quality where two copies of a signal are transmitted in upper and lower sidebands resulting from a single upconversion. *See Bertonis* at col. 9, lns. 47-53. Such signal processing is different than that claimed in the Application. *Rogers* teaches that known image reject mixer circuits were *unsatisfactory* to meet the performance standards required for the applications discussed therein. *See Rogers* at col. 1 lns. 61-64. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 3-4, 20, 23-24, 33, 36-38, 40, and 44-45 be withdrawn.

B. Dependent Claims 12-14, 27-28, and 43

Claims 12-14, 27-28, and 43 each depend either directly or indirectly from Independent Claims 1, 17, and 39 and are thus likewise believed to be allowable at least based on their dependency from Claims 1, 17, and 39 for the reasons discussed above.

1. *Lack of All Claim Limitations*

The combination of *Bertonis* and *Rogers* in further view of Applicants' Admittance or *Cheah* does not teach all claim limitations of Claims 12-14, 27-28, and 43 because none of the references teach the claimed apparatuses and methods adapted to process the signal as described in Claims 12-14, 27-28, and 43. Each of Claims 12-14, 27-28, and 43 limits the claimed apparatus or process from which it depends by imposing a requirement that the apparatus or process be capable of processing an incoming signal having certain components at specific frequencies. The fact that these frequencies are defined (such as by the OPENCABLE standard as described in the Specification at 0006) does not in any way teach or render obvious apparatuses and methods for meeting processing these signals. Indeed, *Bertonis* merely teaches the use of the filter network and image reject mixer of Figure 8 to select the copy of a signal having better quality where two copies of a signal are transmitted in upper and lower sidebands resulting from a single upconversion. *See Bertonis* at col. 9, lns. 47-53. Such signal processing is different than that claimed in the Application. Applicants therefore assert that a prima facie case of obviousness under § 103 has not been made and respectfully request that the rejections of Claims 12-14, 27-28, and 43 be withdrawn.

IV. Summary

In view of the above, the Applicants believe the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 06-2380, under Order No. 49581/P028US/10103789 from which the undersigned is authorized to draw.

Dated: March 2, 2007

Respectfully submitted,

I hereby certify that this document is being transmitted to the US Patent and Trademark Office via electronic filing.

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Exhibit 1

ELECTRIC CIRCUITS

FIFTH EDITION

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PREREQUISITES

In writing the first thirteen chapters of the text, we have assumed that the reader has taken a course in elementary differential and integral calculus. We have also assumed that the reader has had an introductory physics course, at either the high school or university level, which introduced the concepts of energy, power, electric charge, electric current, electric potential, and electromagnetic fields. In writing the final six chapters, we have assumed the student has had, or is enrolled in, an introductory course in differential equations.

COURSE OPTIONS

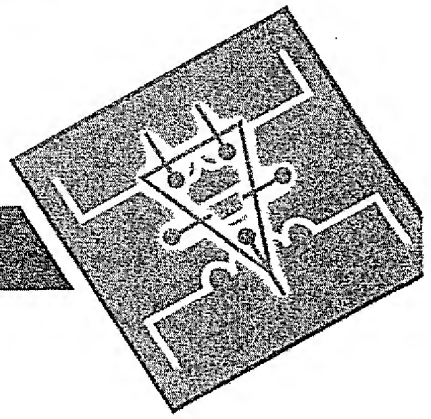
The text has been designed for use in a one-semester, two-semester, or three-quarter sequence.

- *Single-semester course:* After covering Chapters 1–4 and Chapters 6–10, omitting sections 7.7 and 8.5, the instructor can choose from Chapter 5 (operational amplifiers), Chapter 11 (three-phase circuits), Chapter 12 (mutual inductance), and Chapter 17 (Fourier series) to develop the desired emphasis.
- *Two-semester sequence:* Assuming three lectures per week, the first ten chapters can be covered during the first semester, leaving Chapters 11–19 for the second semester.
- *Academic-quarter schedule:* The book can be subdivided into three parts: Chapters 1–7, Chapters 8–13, and Chapters 14–19.

The introduction of operational amplifier circuits can be omitted without interfering with the reading of the subsequent chapters. For example, if Chapter 5 is omitted, the instructor can simply skip Section 7.7, Section 8.5, Chapter 16, and those problems and drill exercises in the chapters following Chapter 5 that pertain to operational amplifiers.

There are several appendixes to help readers make effective use of their mathematical background. Appendix A reviews Cramer's method for solving simultaneous linear equations and simple matrix algebra; complex numbers are reviewed in Appendix B; Appendix C contains the topological foundations for circuit analysis; Appendix D offers a brief discussion of the decibel; Appendix E presents an abbreviated table of trigonometric identities useful in circuit analysis; and an abbreviated table of useful integrals is given in Appendix F. Appendix G provides a comprehensive list of the examples, with titles and corresponding page numbers.

7 RESPONSE OF FIRST-ORDER *RL* AND *RC* CIRCUITS



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In Chapter 6 we noted that an important attribute of inductors and capacitors is their ability to store energy. We are now in a position to determine the currents and voltages that arise when energy is either released or acquired by an inductor or capacitor in response to an abrupt change in a dc voltage or current source. In this chapter, we will focus on circuits that consist only of sources, resistors, and either (but not both) inductors or capacitors. For brevity, such configurations are called *RC* (resistor-capacitor) and *RL* (resistor-inductor) circuits.

Our analysis of *RL* and *RC* circuits will be divided into three phases. In the first phase, we consider the currents and voltages that arise when stored energy in an inductor or capacitor is suddenly released to a resistive network. This happens when the inductor or capacitor is abruptly disconnected from its dc source. Thus we can reduce the circuit to one of the two equivalent forms shown in Fig. 7.1.

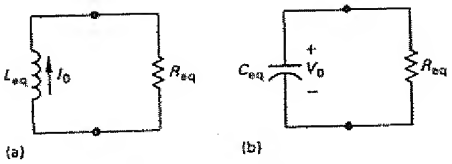

FIGURE 7.1 The two forms of the circuits for natural response: (a) an *RL* circuit; (b) an *RC* circuit.

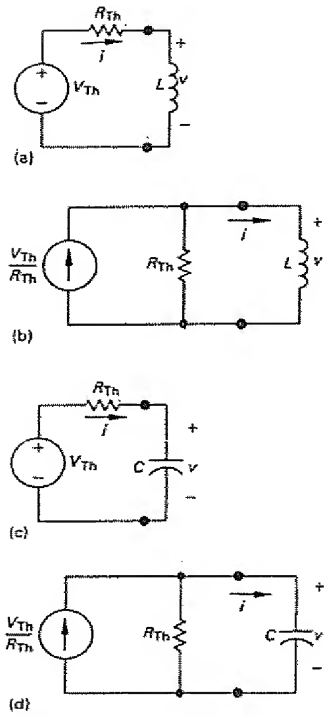

FIGURE 7.2 Four possible first-order circuits: (a) an inductor connected to a Thévenin equivalent; (b) an inductor connected to a Norton equivalent; (c) a capacitor connected to a Thévenin equivalent; (d) a capacitor connected to a Norton equivalent.

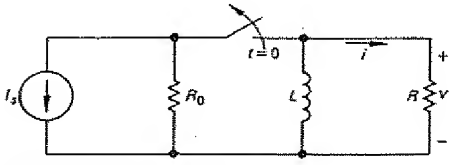

FIGURE 7.3 An *RL* circuit.

The currents and voltages which arise in this configuration are referred to as the **natural response** of the circuit, to emphasize that the nature of the circuit itself, not external sources of excitation, determine its behavior.

In the second phase of our analysis, we consider the currents and voltages that arise when energy is being acquired by an inductor or capacitor due to the sudden application of a dc voltage or current source. This response is referred to as the **step response**. The process for finding both the natural and step responses is the same; thus, in the third phase of our analysis, we develop a general method that can be used to find the response of RL and RC circuits to any abrupt change in a dc voltage or current source.

Figure 7.2 shows the four possibilities for the general configuration of RL and RC circuits. Note that when there are no independent sources in the circuit, the Thévenin voltage or Norton current is zero, and the circuit reduces to one of those shown in Fig. 7.1; that is, we have a natural response problem.

RL and RC circuits are also known as first-order circuits, because their voltages and currents are described by first-order differential equations. No matter how complex a circuit may appear, if it can be reduced to a Thévenin or Norton equivalent connected to the terminals of an equivalent inductor or capacitor, it is a first-order circuit. (Note that if multiple inductors or capacitors exist in the original circuit, they must be interconnected so that they can be replaced by a single equivalent element.)

After introducing the techniques for analyzing the natural and step responses of first-order circuits, we discuss some special cases of interest. The first is that of sequential switching, involving circuits in which switching can take place at two or more instants in time. Next is the unbounded response. Finally, we analyze a useful circuit called the integrating amplifier.

7.1 THE NATURAL RESPONSE OF AN *RL* CIRCUIT

The natural response of an RL circuit can best be described in terms of the circuit shown in Fig. 7.3. We assume that the independent current source generates a constant current of I_s amperes and that the switch has been in a closed position for a long time. We define the phrase *a long time* more accurately later in this section. For now it means that all currents and voltages have reached a constant value. Thus only constant, or dc, currents can exist in the circuit just prior to the switch's being opened, and therefore the inductor appears as a short circuit ($L di/dt = 0$) prior to the release of the stored energy.

Since the inductor appears as a short circuit, the voltage across the inductive branch is zero, and there can be no current in either R_o or R. Therefore all the source current I_s appears in the inductive branch. Finding the natural response requires finding the voltage and current at the terminals of the resistor after the switch has been opened, that is, after the source has been disconnected and the inductor begins releasing energy. If we let $t = 0$ denote the instant when the switch is opened, the problem becomes one of finding $v(t)$ and $i(t)$ for $t \geq 0$. For $t \geq 0$, the circuit shown in Fig. 7.3 reduces to the one shown in Fig. 7.4.

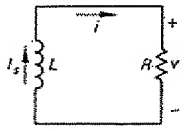

FIGURE 7.4 The circuit shown in Fig. 7.3, for $t \geq 0$.

DERIVING THE EXPRESSION FOR THE CURRENT

To find $i(t)$ we use Kirchhoff's voltage law to obtain an expression involving i, R, and L. Summing the voltages around the closed loop gives

$$L\frac{di}{dt} + Ri = 0, \tag{7.1}$$

where we use the passive sign convention. Equation (7.1) is known as a first-order ordinary differential equation, because it contains terms involving the ordinary derivative of the unknown, that is, di/dt. The highest order derivative appearing in the equation is 1; hence the term **first-order**.

You can use a symbolic equation solver to find the closed-form solution for this first-order equation.

We can go one step farther in describing this equation. The coefficients in the equation, R and L, are constants; that is, they are not functions of either the dependent variable i or the independent variable t. Thus the equation can also be described as an ordinary differential equation with constant coefficients.

To solve Eq. (7.1), we divide through by L, transpose the term involving i to the right-hand side, and then multiply both sides by a differential time dt. The result is

$$\frac{di}{dt}dt = -\frac{R}{L}idt. \tag{7.2}$$

Next, we recognize the left-hand side of Eq. (7.2) as a differential change in the current i, that is, di. We now divide through by i, getting

$$\frac{di}{i} = -\frac{R}{L}dt. \tag{7.3}$$

We obtain an explicit expression for i as a function of t by integrating both sides of Eq. (7.3). Using x and y as variables of integration yields

$$\int_{i(t_0)}^{i(t)} \frac{dx}{x} = -\frac{R}{L}\int_{t_0}^{t} dy, \tag{7.4}$$

in which $i(t_0)$ is the current corresponding to time t_0, and $i(t)$ is the

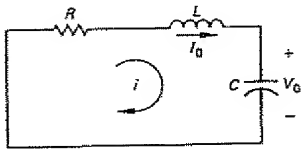

FIGURE 8.3 A circuit used to illustrate the natural response of a series *RLC* circuit.

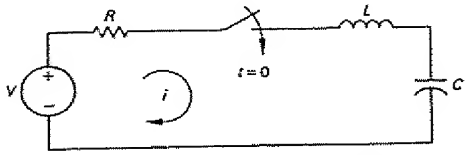

FIGURE 8.4 A circuit used to illustrate the step response of a series *RLC* circuit.

Finding the natural response of a series *RLC* circuit consists of finding the current generated in the series-connected elements by the release of initially stored energy in the inductor, capacitor, or both. The task is defined by the circuit shown in Fig. 8.3. As before, the initial inductor current, I_0, and the initial capacitor voltage, V_0, represent the initially stored energy. If any of the individual element voltages are of interest, you can find them after determining the current.

We describe the step response of a series *RLC* circuit in terms of the circuit shown in Fig. 8.4. We are interested in the current resulting from the sudden application of the dc voltage source. Energy may or may not be stored in the circuit when the switch is closed.

If you have not studied ordinary differential equations, derivation of the natural and step responses of parallel and series *RLC* circuits may be a bit difficult to follow. However, the results are important enough to warrant presentation at this time. We begin with the natural response of a parallel *RLC* circuit and cover this material over two sections: one to discuss the solution of the differential equation that describes the circuit, and one to present the three distinct forms that the solution can take. After introducing these three forms, we show that the same forms apply to the step response of a parallel *RLC* circuit, as well as to the natural and step responses of series *RLC* circuits.

8.1 INTRODUCTION TO THE NATURAL RESPONSE OF A PARALLEL *RLC* CIRCUIT

The first step in finding the natural response of the circuit shown in Fig. 8.1 is to derive the differential equation that the voltage v must satisfy. We choose to find the voltage first, because it is the same for each component. After that, a branch current can be found by using the current-voltage relationship for the branch component. We easily obtain the differential equation for the voltage by summing the currents away from the top node, where each current is expressed as a function of the unknown voltage v:

$$\frac{v}{R} + \frac{1}{L}\int_0^t v\,d\tau + I_0 + C\frac{dv}{dt} = 0. \tag{8.1}$$

We eliminate the integral in Eq. (8.1) by differentiating once with respect to t, and, because I_0 is a constant, we get

$$\frac{1}{R}\frac{dv}{dt} + \frac{v}{L} + C\frac{d^2v}{dt^2} = 0. \tag{8.2}$$

We now divide through Eq. (8.2) by the capacitance C and arrange

the derivatives in descending order:

$$\frac{d^2v}{dt^2} + \frac{1}{RC}\frac{dv}{dt} + \frac{v}{LC} = 0. \tag{8.3}$$

Comparing Eq. (8.3) with the differential equations derived in Chapter 7 reveals that they differ by the presence of the term involving the second derivative. Equation (8.3) is an ordinary, second-order differential equation with constant coefficients. Circuits in this chapter contain both inductors and capacitors, so the differential equation describing these circuits is of the second order. Therefore, we sometimes call such circuits **second-order circuits.**

You can use a symbolic equation solver to find closed-form solutions for second-order differential equations.

THE GENERAL SOLUTION OF THE SECOND-ORDER DIFFERENTIAL EQUATION

We can't solve Eq. (8.3) by separating the variables and integrating as we were able to do with the first-order equations in Chapter 7. The classical approach to solving Eq. (8.3) is to assume that the solution is of exponential form, that is, to assume that the voltage is of the form

$$v = Ae^{st}, \tag{8.4}$$

where A and s are unknown constants.

Before showing how this assumption leads to the solution of Eq. (8.3), we need to show that it is rational. The strongest argument we can make in favor of Eq. (8.4) is to note from Eq. (8.3) that the second derivative of the solution, plus a constant times the first derivative, plus a constant times the solution itself, must sum to zero for all values of t. This can occur only if higher order derivatives of the solution have the same form as the solution. The exponential function satisfies this criterion. A second argument in favor of Eq. (8.4) is that the solutions of all the first-order equations we derived in Chapter 7 were exponential. It seems reasonable to assume that the solution of the second-order equation also involves the exponential function.

If Eq. (8.4) is a solution of Eq. (8.3), it must satisfy Eq. (8.3) for all values of t. Substituting Eq. (8.4) into Eq. (8.3) generates the expression

$$As^2e^{st} + \frac{As}{RC}e^{st} + \frac{Ae^{st}}{LC} = 0,$$

or

$$Ae^{st}\left(s^2 + \frac{s}{RC} + \frac{1}{LC}\right) = 0, \tag{8.5}$$

which can be satisfied for all values of t only if A is zero or the parenthetical term is zero, because $e^{st} \neq 0$ for any finite values of st. We cannot use $A = 0$ as a general solution because to do so implies that the voltage is zero for all time—a physical impossibility if energy is stored in either the inductor or capacitor. Therefore, in order